DP-303087

SELF TESTING CMOS IMAGER CHIP

ABSTRACT OF THE DISCLOSURE

A self testing CMOS imager chip includes a controller which outputs a sewer signal, a dump signal, a collect signal, and a read signal, and a pixel array connected to the controller including a plurality of pixels arranged in an array of rows and columns, each pixel having a collect gate disposed adjacent a collect well for receiving a charge in response to application of the collect signal to the collect gate, a sewer for injecting a charge into the collect well in response to the concurrent application of the sewer signal to the sewer and the collect signal to the collect well, a read gate disposed adjacent a read well for receiving the injected charge from the collect well in response to application of the read signal to the read gate and the absence of the collect signal at the collect gate, and a transistor having a gate coupled to the read well, a source for receiving the read signal, and a drain coupled to an output node connected to the controller. The read signal is modulated by the injected charge at the gate of the transistor, thereby generating an injected output signal at the output node representing the injected charge. The controller, through read-out circuitry, comparing the injected output signal to an expected output signal to test the operation of each pixel of the array.